SELECTING A/D CONVERTERS

One of the popular pastimes of the nineteen sixties was to predict the explosive growth of digital data processing, fed by the newly-developed semiconductor MSI circuits, and the subsequent demise of analog circuitry. The first part of this prediction has certainly come true - the advent of the microprocessor has caused, and will continue to cause, a revolution in digital processing which was unthinkable 10 years ago. But far from causing the demise of analog systems, the reverse has occurred. Nearly all the data being processed (with the notable exception of financial data) consists of physical parameters of an analog nature - pressure, temperature, velocity, light intensity and acceleration to name but a few. In every instance this analog information must be converted into its digital equivalent, using some form of A/D converter. Converter products are thus assuming a key role in the realization of data acquisition systems.

Increased use of microprocessors has also caused dramatic cost reductions in the digital components of a typical system. The $8000 mini-computer of a few years ago is being replaced by a $475 dedicated microprocessor board. This trend is also being reflected in the analog components. No longer is it possible to justify buying a $400 data acquisition module when a dedicated system, adequate for the task under consideration, can be put together for $50.

Thus many engineers, who in the past have had limited exposure to analog circuitry, are having to come to grips with the characteristics of A/D converters, sample & holds, multiplexers and operational amplifiers. Contrary to the propaganda put out by many of the specialty module houses, there is nothing mysterious about these components or the way they interface with one another. Now that many of them are available as one or two chip MSI circuits, a block diagram may be turned into a working piece of hardware with relative ease.

The purpose of this note is to compare and contrast the more popular A/D designs, and provide the reader with sufficient information to select the most appropriate converter for his or her needs.

THE IMPORTANT PARAMETERS

Let's begin by taking a look at some actual systems, since this will illustrate the diversity of performance required of A-to-D converters.

Case 1: A seismic recording truck is situated over a potential natural gas site. Some 32 recording devices are laid out over the surrounding area. An explosive charge is detonated and in a matter of seconds it is all over. During that time it is necessary to scan each recorder every 100 microseconds. Speed is clearly the most important requirement. In this instance, 12 bit accuracy is not required; and, since the truck contains many thousands of dollars of electronics, cost is not a critical parameter. The A/D will be a high speed successive approximation design.

Case 2: A semiconductor engineer is measuring the 'thermal profile' of a furnace. It is necessary to make measurements accurate to a few tenths of a degree Centigrade, which is equivalent to a few microvolts of thermocouple output. Sampling rates of a few readings per second are adequate and costs should be kept low. The integrating ('dual slope', 'triphasic', 'quad slope', depending on which manufacturer you go to) A/D is the only type capable of the required precision/cost combination. It has the added advantage of maintaining accuracy in a noisy environment.

Case 3: A businessman is talking to his sales office in Rome. Assuming the phone company is not on strike, his voice will be sampled at a 10KHz rate, or thereabouts, in order not to lose information in the audio frequency range up to 5KHz. This requires a medium accuracy (8 bit) A/D with a cycle time of 100 microseconds or less. In this application the integrating type is not fast enough, so it is necessary to use a slow (for this approach) successive approximation design.

These examples serve to introduce both the two most popular conversion techniques (successive approximation and integrating) and the three key parameters of a converter, i.e. speed, accuracy and cost. In fact the first choice in selecting an A/D is between successive approximation and integrating, since greater than 95% of all converters fall into one of these two categories.

If we look at the whole gamut of available converters, with conversion speeds ranging from 100 ms to less than 1 μs, we see that these two design approaches divide the speed spectrum into two groups with almost no overlap. (Table 1) However, before making a selection solely on the basis of speed, it is important to have an understanding of how the converters work, and how the data sheet specifications relate to the circuit operation.

TABLE 1

Type of converter	Relative speed	Conversion time 8 bits	10 bits	12 bits	16 bits
integrating	slow	20 ms	30 ms	40 ms	250 ms
	medium	1 ms	5 ms	20 ms	—
	fast	0.3 ms	1 ms	5 ms	—
successive approximation	general purpose	30 μs	40 μs	50 μs	—
	high performance	10 μs	15 μs	20 μs	400 μs
	fast	5 μs	10 μs	12 μs	—
	high speed	2 μs	4 μs	6 μs	—
	ultra-fast	0.8 μs	1 μs	2 μs	—

THE INTEGRATING CONVERTER

Summary of Characteristics

As the name implies, the output of an integrating converter represents the integral or average value of an input voltage over a fixed period of time. A sample-and-hold circuit, therefore, is not required to freeze the input during the measurement period, and noise rejection is excellent. Equally important, the linearity error of integrating converters is small since they use time to quantize the answer - it is relatively easy to hold short-term clock jitter to better than 1 in 10^6.

The most popular integrating converter uses the dual-slope principle, a detailed description of which is given in Ref. 1.

Its advantages and disadvantages may be summarized as follows:

Advantages:

- Inherent accuracy
- Non-critical components
- Excellent noise rejection
- No sample & hold required
- Low cost
- No missing codes

Disadvantages:

- Low speed (typically 3 to 100 readings/sec)

In a practical circuit, the primary errors (other than reference drift) are caused by the non-ideal characteristics of analog switches and capacitors. In the former, leakage and charge injection are the main culprits; in the latter, dielectric absorption is a source of error. All these factors are discussed at length in Ref. 1.

A well-designed dual slope circuit such as Intersil's 8052A/7103A is capable of 4½ digit performance (±1 in ±20,000) with no critical tweaks or close tolerance components other than a stable reference.

Timing Considerations

In a typical circuit, such as the 8052A/7103A referred to above, the conversion takes place in three phases as shown in Fig 1. Note that the input is actually integrated or averaged over a period of 10,000 clock pulses (or 83.3 ms with a 120 KHz clock) within a conversion cycle of 40,000 clock pulses in toto. Also note that the actual business of looking at the input signal does not begin for 10,000 clock pulses, since the circuit first goes into an auto-zero mode. For a 3½ digit product, such as the 7101 or 7103, the measurement period is 1000 clock pulses (or 8.33 ms with a 120 KHz clock).

These timing characteristics give the dual slope circuit both its strengths and its weaknesses. By making the signal integrate period an integral number of line frequency periods, excellent 60Hz noise rejection can be obtained. And of course integrating the input signal for several milliseconds smoothes out the effect of high frequency noise.

But in many applications such as transient analysis or sampling high frequency waveforms, averaging the input over several milliseconds is totally unacceptable. It is of course feasible to use a sample & hold at the input, but the majority of systems that demand a short measurement window also require high speed conversions.

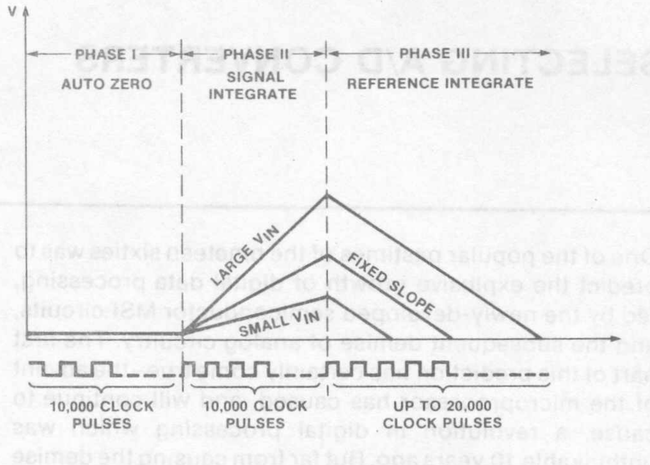


Figure 1: 4½ Digit A/D Converter Timing Diagram (8052A/7103A)

THE SUCCESSIVE APPROXIMATION CONVERTER

How it works.

The heart of the successive approximation A/D is a digital-to-analog converter (DAC) in a feedback loop with a comparator and some clever logic referred to as a 'successive approximation register' (SAR). Fig 2 shows a typical system. The DAC output is compared with the analog input, progressing from the most significant bit (MSB) to the least significant bit (LSB) one bit at a time. The bit in question is set to one. If the DAC output is less than the input, the bit in question is left at one. If the DAC output is greater than the input, the bit is set to zero. The register then moves on to the next bit. At the completion of the conversion, those bits left in the one state cause a current to flow at the output of the DAC which should match I_{IN} within ± ½ LSB. Performing an 'n' bit conversion requires only 'n' trials, making the technique capable of high speed conversion.

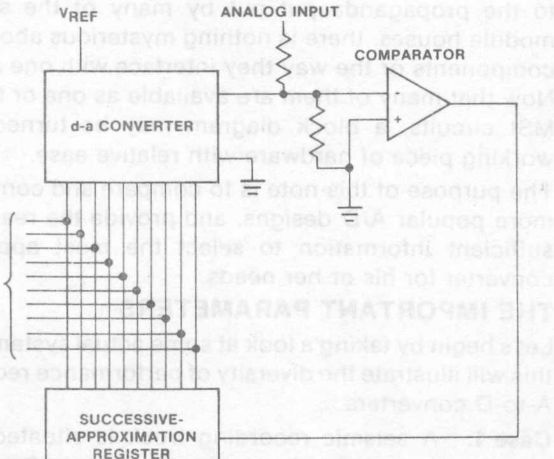


Figure 2: Successive Approximation A/D Converter

The advantages and disadvantages of successive approximation converters may be summarized as follows:

Advantages:

- Hi Speed (Typically 100,000 conversions/sec)

Disadvantages:

- Several critical components
- Can have missing codes
- Requires sample and hold
- Difficult to auto-zero
- High cost

Error Sources

The error source in the successive approximation converter are more numerous than in the integrating type, with contributions from both the DAC and the comparator. The DAC generally relies on a resistor ladder and current or voltage switches to achieve quantization. Maintaining the correct impedance ratios over the operating temperature range is much more difficult than maintaining clock pulse uniformity in an integrating converter.

The data sheet for a hypothetical A/D might contain the following accuracy related specifications:

Resolution	:	10 Bits
Quantization Uncertainty	:	± ½ LSB
Relative Accuracy	:	± ½ LSB
Differential Non Linearity	:	± ½ LSB
Gain Error	:	Adjustable to zero at 25°C
Gain Temp. Coeff.	:	± 10 ppm of Full Scale Reading /°C
Offset Error	:	Adjustable to zero at 25°C
Offset Temp. Coeff.	:	± 20 ppm of Full Scale Reading /°C

Now, referring to the definition of terms on page 6, what does this tell us about the product? First of all, being told that the *quantization uncertainty* is ± ½ LSB is like being told that binary numbers are comprised of ones and zeros - it's part of the system. The *relative accuracy* of ± ½ LSB, guaranteed over the temperature range, tells us that after removing gain and offset errors, the transfer function never deviates by more than ± ½ LSB from where it should be. That's a good spec., but note that gain and offset errors have been adjusted prior to making the measurement. Over a finite temperature range, the temperature coefficients of gain and offset must be taken into account.

The *differential non-linearity* of ± ½ LSB maximum is also guaranteed over temperature: this ensures that there are no missing codes.

The *gain temperature coefficient* is 10 ppm of FSR per °C, or 0.001% per °C. Now 1 LSB in a 10 bit system is 1 part in 1024, or approximately 0.1%. So a 50°C temperature change from the temperature at which the gain was adjusted (i.e. from +25°C to +75°C) could give rise to ± ½ LSB error. This error is separate from, and in the limit could add to, the relative accuracy spec.

The *offset temperature coefficient* of 20 ppm per °C give rise to ± 1 LSB error (over a +25°C to +75°C range) by the same reasoning applied to the gain tempco. The reference contributes an error in direct proportion to its percentage change over the operating temperature range.

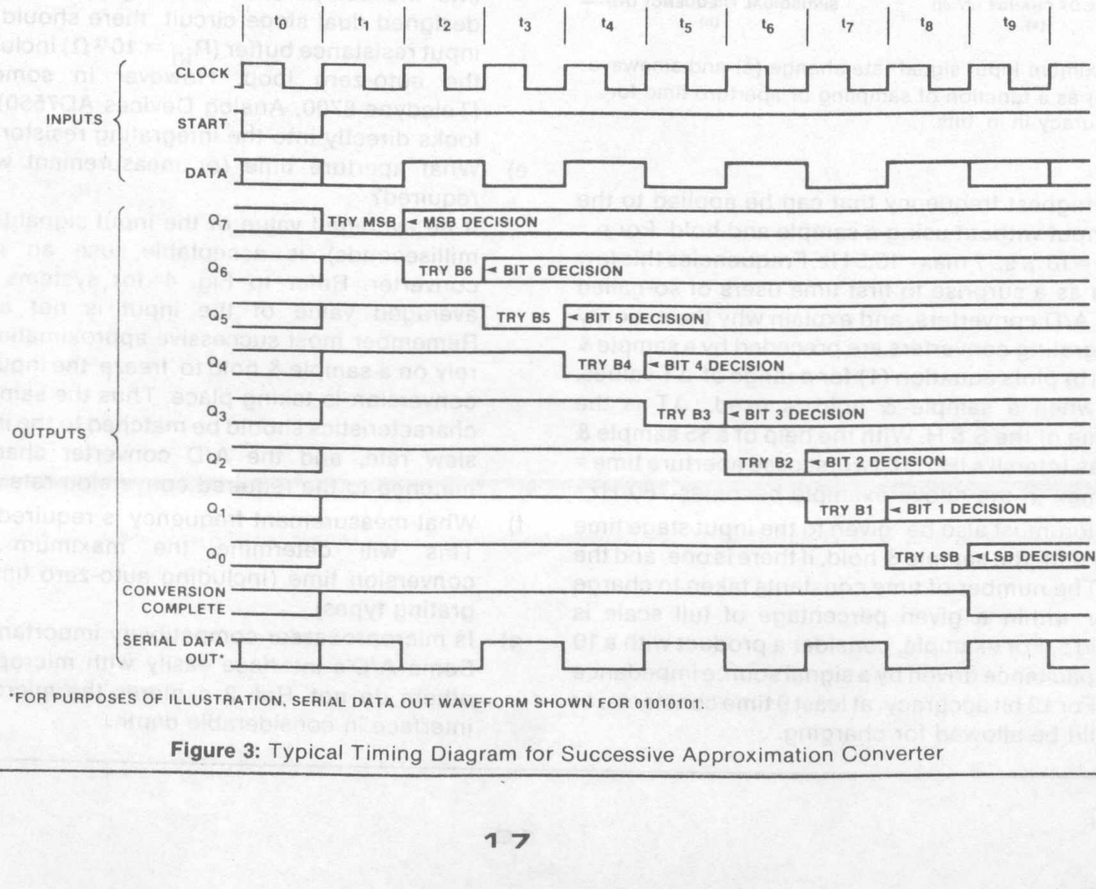
We can summarize the effect of the major error sources:

Relative Accuracy	± ½ LSB or ± .05%
Gain Temp. Coefficient	± ½ LSB or ± .05%
Offset Temp. Coefficient	± 1 LSB or ± 0.1%

A straight forward RMS summation shows that the A/D is 10 bits ± 1¼ LSB over a 0°C to +75°C temperature range. However it is over-optimistic to RMS errors with such a small number of variables, and yet we do know that the error cannot exceed ± 2 LSB. A realistic estimate might place the accuracy at 10 bits ± 1½ LSB.

Timing Considerations

The 2502/2503/2504 successive approximation register is now used in the majority of high speed A/D converters and the timing diagram shown in Fig. 3 is taken from the



*FOR PURPOSES OF ILLUSTRATION, SERIAL DATA OUT WAVEFORM SHOWN FOR 01010101.

Figure 3: Typical Timing Diagram for Successive Approximation Converter

2502 data sheet. However all successive approximation converters have essentially similar timing characteristics. Holding the start input Low for at least a clock period initiates the conversion. The MSB is set low and all the other bits high for the first trial. Each trial takes one clock period, proceeding from the MSB to the LSB. Note that, in contrast to the integrating converter, a serial output arises naturally from this conversion technique.

Although the successive approximation A/D is capable of very high conversion speeds, there is an important limitation on the slew rate of the input signal. Unlike integrating designs, no averaging of the input signal takes place. To maintain accuracy to 10 bits, for example, the input should not change by more than ± ½ LSB during the conversion period. Fig 4(a) shows maximum allowable dV/dt as a function of sampling (or aperture) time for various conversion resolutions. Now for a sinusoidal waveform represented by $E\sin\omega t$, the maximum rate of change of voltage $\Delta e/\Delta t$ is $2\pi f E$. The amplitude of one ½ LSB is $E/2^n$, since the pk-pk amplitude is 2E. So the change in input amplitude Δe is given by:

$$\Delta e = E/2^n = 2\pi f E \Delta T, \text{ where } \Delta T = \text{conversion time}$$

$$f\max = \frac{1}{2\pi \Delta T 2^n}$$

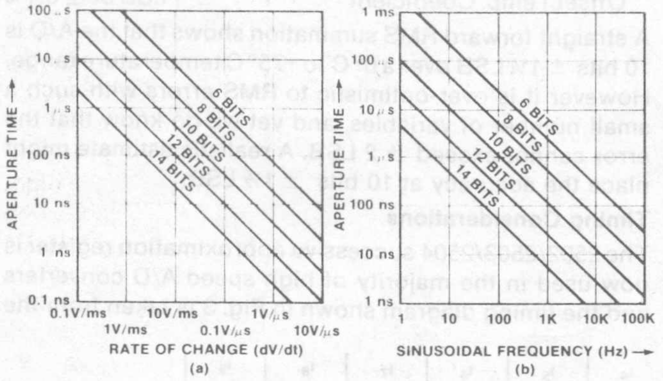


Figure 4: Maximum input signal rate change (a) and sinewave frequency (b) as a function of sampling or aperture time for ± ½ LSB accuracy in 'n' bits.

This is the highest frequency that can be applied to the converter input without using a sample and hold. For n = 10 bits, $\Delta T = 10\ \mu s$, $f\max = 15.5$ Hz. Frequencies this low often come as a surprise to first time users of so-called high speed A/D converters, and explain why the majority of non-integrating converters are preceded by a sample & hold. Fig. 4(b) plots equation (1) for a range of ΔT values. Note that when a sample & hold is used, ΔT is the aperture time of the S & H. With the help of a $5 sample & hold such as Intersil's IH5110 (worst case aperture time = 200 ns), $f\max$ in the above example becomes 780 Hz.

Consideration must also be given to the input stage time constant of both the sample & hold, if there is one, and the converter. The number of time constants taken to charge a capacitor within a given percentage of full scale is shown in Fig 5. For example, consider a product with a 10 pF input capacitance driven by a signal source impedance of 100K Ω. For 12 bit accuracy, at least 9 time constants, or 9 μs, should be allowed for charging.

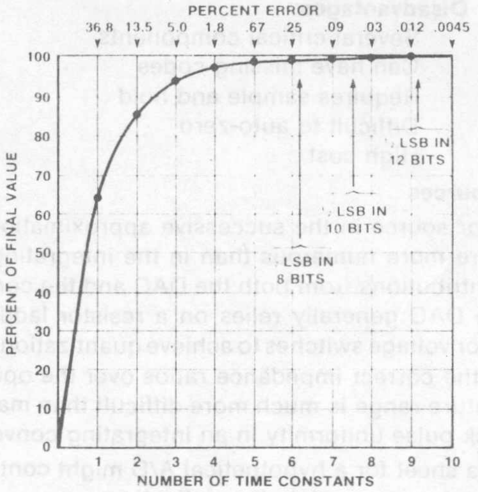


Figure 5: Voltage across a capacitor (as % of final value) as a function of time (# of time constants)

CONVERTER CHECKLIST

In selecting a converter for a specific application, it will be helpful to go through the following checklist, matching required performance against data sheet guarantees:

a) How many bits?

b) What is total error budget over the temperature range?

c) What is full scale reading and magnitude of LSB? Make sure that the 95% noise is substantially less than the magnitude of the LSB. If no noise specifications are given, assume that the omission is intentional!

d) What input characteristics are required? With most successive approximation converters, the input resistance is low (≃ 5KΩ) since one is looking into the comparator summing junction. In a well designed dual slope circuit, there should be a high input resistance buffer ($R_{in} \simeq 10^{12}\ \Omega$) included within the auto-zero loop. However in some designs (Teledyne 8700, Analog Devices AD7550) the input looks directly into the integrating resistor (1 MΩ).

e) What aperture time (or measurement window) is required? If an averaged value of the input signal (over some milliseconds) is acceptable, use an integrating converter. Refer to Fig. 4 for systems where an averaged value of the input is not acceptable. Remember most successive approximation systems rely on a sample & hold to 'freeze' the input while the conversion is taking place. Thus the sample & hold characteristics should be matched to the input signal slew rate, and the A/D converter characteristics matched to the required conversion rate.

f) What measurement frequency is required? This will determine the maximum allowable conversion time (including auto-zero time for integrating types).

g) Is microprocessor compatibility important? Some A/D's interface easily with microprocessors; others do not. Ref. 2 explores the microprocessor interface in considerable depth.

h) Does the converter form part of a multiplexed data acquisition system?
Note that some integrating converters (Motorola MC14433) assess polarity based on the input voltage during the previous conversion cycle. Such designs are clearly unsuitable for multiplexed inputs where the signal polarity bears no relationship to the previously measured value. They can also give trouble with inputs hovering around zero.

i) Is 60Hz rejection important?
If the line frequency rejection capabilities of the integrating converter are important, make sure that the duration of the measurement (input integrate) period is a fixed number of clock pulses. In some designs, the input integration time is programmed by the auto-zero information, making rejection of specific frequencies impossible.

MULTIPLEXED DATA SYSTEMS

The foregoing discussion has summarized the characteristics of A/D converters as stand-alone components. However, one of the most important applications for A/Ds is as part of a multiplexed data acquisition system. Traditionally, systems of this type have used analog signal transmission between the transducer and a central multiplexer/converter console. (Fig 6a) To sample 100 data points 25 times per second requires a 100 input analog multiplexer and an A/D capable of 2500 conversions per second. A successive approximation converter would be the obvious choice.

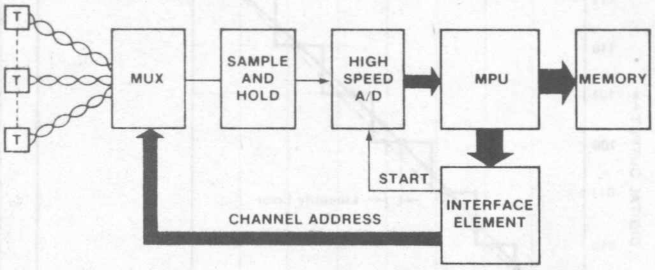


Figure 6(a): Data Acquisition using one central A/D.

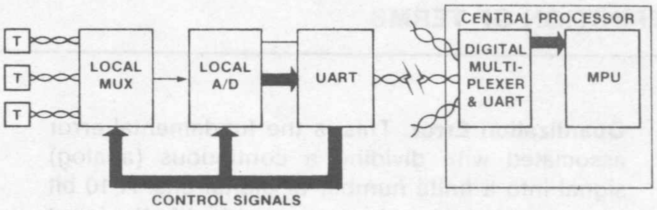


Figure 6(b): Data Acquisition using several local A/Ds

Another approach, which becomes attractive with the availability of low cost IC converters, is to use localized A/D conversion with digital transmission back to a central console. In the limit one could use a converter per transducer, but it is often more economical to have a local conversion station servicing several transducers (Fig 6b). Several advantages result from this approach. Firstly, digital transmission is more satisfactory in a noisy environment, and lends itself to optical isolation techniques better than analog transmission. Secondly, using local conversion stations significantly reduces the number of interconnects back to the central processor. When one considers that the instrumentation for a typical power plant uses 4.5 million feet of cable, this can result in real cost savings. Finally, by sharing the conversion workload among several A/Ds, it is frequently possible to switch from a successive approximation to a dual slope design.

An example of a local conversion station featuring an 8052/7103 dual slope A/D, a CMOS multiplexer, and an UART for serial data transmission is discussed in Ref 2. The local conversion station concept can be taken a stage further by the addition of a microprocessor. This may be used to reduce the data prior to transmission to the central computer, and/or to look for dangerous conditions, for example.

REFERENCES:

(1) Intersil Application Bulletin A017, "The Integrating A/D Converter," by Lee Evans.

(2) Peter Bradshaw et al., "Interfacing Data Converters and Microprocessors," Electronics, Dec. 9, 1976.

(3) Intersil Application Bulletin A018, "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.

DEFINITION OF TERMS

Quantization Error. This is the fundamental error associated with dividing a continuous (analog) signal into a finite number of digital bits. A 10 bit converter, for example, can only identify the input voltage to 1 part in 2^{10}, and there is an unavoidable output uncertainty of $\pm$ ½ LSB (Least Significant Bit). See Fig. 7.

Linearity. The maximum deviation from a straight line drawn between the end points of the converter transfer function. Linearity is usually expressed as a fraction of LSB size. The linearity of a good converter is $\pm$ ½ LSB. See Fig. 8.

Differential Non-Linearity. This describes the variation in the analog value between adjacent pairs of digital numbers, over the full range of the digital output. If each transition is equal to 1 LSB, the differential non-linearity is clearly zero. If the transition is 1 LSB $\pm$ ½ LSB, then there is a differential linearity error of $\pm$ ½ LSB, but no possibility of missing codes. If the transition is 1 LSB $\pm$ 1 LSB, then there is the possibility of missing codes. This means that the output may jump from, say 011 . . . . 111 to 100 . . . . 001, missing out 100 . . . . 000. See Fig. 9.

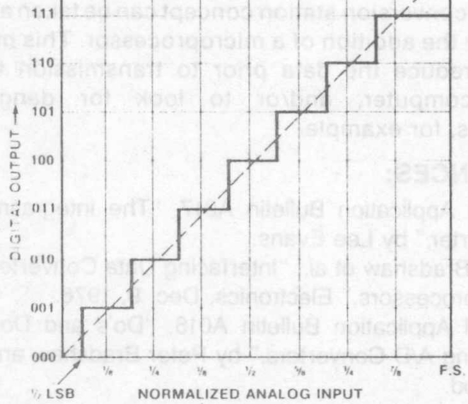


Figure 7: Ideal A/D conversion

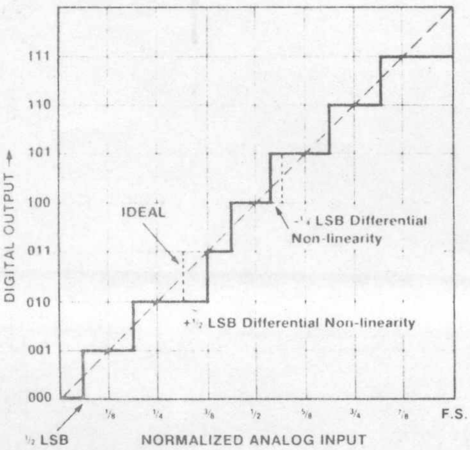


Figure 9: Differential Non-linearity

Relative Accuracy. The input to output error as a fraction of full scale, with gain and offset errors adjusted to zero. Relative accuracy is a function of linearity, and is usually specified at less than $\pm$ ½ LSB.

Gain Error. The difference in slope between the actual transfer function and the ideal transfer function, expressed as a percentage. This error is generally adjustable to zero by adjusting the input resistor in a current-comparing successive approximation A/D. See Fig. 10.

Gain Temperature Coefficient. The deviation from zero gain error on a 'zeroed' part which occurs as the temperature moves away from 25°C. See Fig. 10.

Offset Error. The mean value of input voltage required to set zero code out. This error can generally be trimmed to zero at any given temperature, or is automatically zeroed in the case of a good integrating design.

Offset Temperature Coefficient. The change in offset error as a function of temperature.

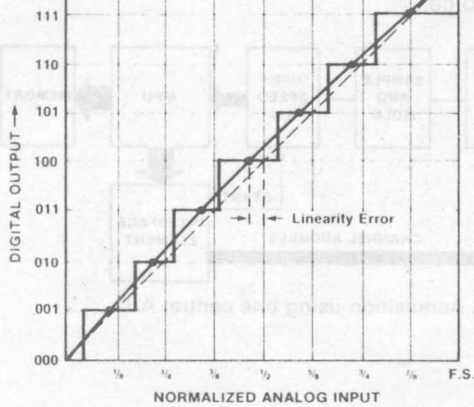


Figure 8: Linearity Error

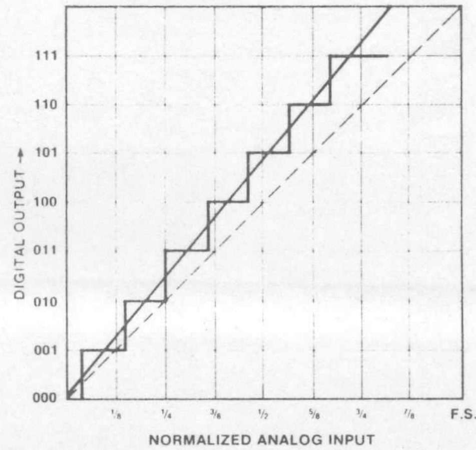


Figure 10: Gain Error